Amendments to the Claims

1. CURRENTLY AMENDED) A semiconductor device having a first major surface; comprising: at least one cell ~~(18)~~ having longitudinally spaced source and drain regions ~~(22, 24)~~ at the first major surface ~~(16)~~, a source body region ~~(26)~~ at the end of the source region ~~(22)~~ facing the drain region ~~(24)~~, a drain body region ~~(28)~~ at the end of the drain region ~~(24)~~ facing the source region ~~(22)~~ and a drift region ~~(20)~~ extending from the source body region ~~(26)~~ to the drain body region ~~(28)~~;

at least one pair of longitudinally spaced insulated gates ~~(31)~~, one of the pair being adjacent to the source body region ~~(26)~~ and the other of the pair being adjacent to the drain body region ~~(28)~~, the gates extending longitudinally with longitudinal side walls, the insulated gates being formed in trenches having gate dielectric ~~(3)~~ along the side and end walls and the base of the trench and a gate conductor within the gate dielectric; and

plates ~~(33, 50)~~ adjacent to the drift region ~~(20)~~ for controlling the drift region ~~(20)~~ to carry current flowing between source amd drain ~~(22, 24)~~ when the device is switched on and to support a voltage between source and drain ~~(22, 24)~~ when the device is switched off.

2. (CURRENTLY AMENDED) A semiconductor device according to claim 1 wherein the source and drain regions ~~(22,24)~~ are of a first conductivity type and the source and drain body regions are of a second conductivity type ~~(26,28)~~ opposite to the first conductivity type.

3. (CURRENTLY AMENDED) A semiconductor device according to claim 2 wherein the drift region ~~(20)~~ is of the first conductivity type with a dopant concentration in the range of 5×10^{16} cm $^{-3}$ to 5×10^{17} cm^{-3},

4. (CURRENTLY AMENDED) A semiconductor device according to ~~any preceding claim~~claim 1 wherein the plates are insulated conductive potential plates ~~(23)~~ adjacent to the drift region.

5. (CURRENTLY AMENDED) A semiconductor device according to claim 4 wherein an insulated conductive potential plate ~~(33)~~ extends from the each of the pair ~~(30)~~ of gates longitudinally towards the other of the pair of gates adjacent to the drift region ~~(20)~~, each conductive potential plate ~~(33)~~ being in electrical contact with the gate ~~(31)~~ from which it extends.

6. (CURRENTLY AMENDED) A semiconductor device according to claim 5 wherein the dielectric ~~(32)~~ along the side wall of the potential plates ~~(33)~~ has a greater thickness than the dielectric ~~(32)~~ along the side wall of the gates ~~(31)~~.

7. (CURRENTLY AMENDED) A semiconductor device according to claim 4 comprising at least one longitudinally extending potential plate ~~(33)~~ between the longitudinally spaced gates ~~(31)~~ and insulated from the longitudinally spaced gates ~~(31)~~.

8. (CURRENTLY AMENDED) A semiconductor device according to ~~any preceding claim~~claim 1 comprising 81 plurality of cells ~~(18)~~ spaced laterally across the first major surface of the substrate alternating with pairs ~~(30)~~ of longitudinally spaced insulated gates.

9. (CURRENTLY AMENDED) A semiconductor device according to ~~claim 1 or 2~~ claim 1 wherein the plates comprise resistive field plates ~~(50)~~ extending longitudinally on either side of the or each cell ~~(18)~~ from a source end adjacent to the source ~~(22)~~ to a drain end adjacent to the drain ~~(24)~~ laterally on either side of the or each cell ~~(18)~~.

10. (CURRENTLY AMENDED) A semiconductor device according to claim 9 further comprising a source contact ~~(40)~~ connected in common to the source region or regions ~~(22)~~ and to the source end of the field plate or plates ~~(50)~~ and a drain contact ~~(42)~~ connected in common to the drain region or regions ~~(24)~~ and drain end the field plate or plates ~~(50)~~.

11. (CURRENTLY AMENDED) A semiconductor device according to ~~claim 9 or 10~~ claim 9 wherein the gate trenches ~~(35)~~ extend from the first major surface to the substrate and the semi-insulating field plates each extend from the first major surface to the substrate.

12. (CURRENTLY AMENDED) A semiconductor device according to ~~any of claims 9 to 11~~ claim 9 including a plurality of cells ~~(18)~~ and field plates ~~(50)~~ alternating laterally across the first major surface ~~(16)~~.

13. (CURRENTLY AMENDED) A semiconductor device according to ~~any preceding claim~~ claim 1 wherein the gates ~~(31)~~ are arranged within the lateral bounds of each cell.

14. (CURRENTLY AMENDED) A semiconductor device according to ~~any preceding claim~~ claim 1 wherein the source body region ~~(26)~~ extends under the source region (22) and the drain body region ~~(28)~~ extends under the drain region ~~(24)~~.

15. (CURRENTLY AMENDED) A semiconductor device according to ~~any preceding claim~~ claim 1 comprising a source contact ~~(40)~~ connected in common to the source ~~(22)~~ and to the source body region ~~(26)~~ alnd a drain contact ~~(42)~~ connected in common to the drain ~~(24)~~ and the drain body rrsgion ~~(28)~~.